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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,760	10/24/2003	Yuan-Liang Wu	CMOP0026USA	2759

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EXAMINER	
CHOW, DOON Y	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,760	WU ET AL.	
	Examiner	Art Unit	
	Dennis-Doon Chow	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-19* is/are allowed.

6)☒ Claim(s) *1-4,12 and 13* is/are rejected.

7)☒ Claim(s) *5-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Adachi (JP401319094).

Regarding to claims 1, Adachi discloses a driving circuit of a liquid crystal display device comprising: a substrate (101, Fig. 7); at least two driver integrated circuit (IC) chips (101, 109, Fig. 1) positioned on the substrate; and an impedance device (206, 207, 208, Fig. 3) electrically connected between the two driver IC chips. The inpedcance device inherently reduces a difference between respective input voltages being input into the two driver IC chips.

Regarding to claim 2, Adachi discloses the substrate comprises a plurality of scanning lines (122, Fig. 8) and a plurality of signal lines thereon (119, Figs. 1 and 8).

Regarding to claim 4, the driver IC chips are used for outputting image signals to the signal lines (see Figs. 1 and 8).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi in view of applicant's admitted prior art..

Regarding to claim 3, Adachi does not explicitly disclose connecting diver circuits (driver IC chips) to the scanning lines.

The admitted prior art discloses connecting a plurality of driver IC chips (22, Fig.1) to a plurality of scanning lines.

In light of the admitted prior art, it would have been obvious to one of ordinary skill in the art to connect the IC ships to Adachi's scanning lines because there must be driver circuits for driving the scanning lines.

Regarding to claim 13, Adachi does not disclose the liquid crystal display device is designed by applying wiring on array (WOA) technology.

The admitted prior art disclose a liquid crystal display device is designed by applying wiring on array (WOA) technology to reduce a production cost [0008].

In light of the admitted prior art, it would have been obvious to one of ordinary skill in the art to apply the wiring on array (WOA) technology on Adachi' s liquid crystal display device to reduce a production cost.

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi.

Adachi further discloses a conductive layer is positioned between each of the driver IC chips and the impedance device (see connections in Fig. 3), each of the driver IC chips being capable of receiving an approximately identical input voltage through each of the transparent conductive layers. Adachi does not disclose the conductive layer is transparent. However, it is considered a matter of obvious design choice to make Adachi's conductive layer transparent because this does not provide any unexpected result.

Allowable Subject Matter

6. Claims 5-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 14-19 are allowed.

Response to Arguments

8. Applicant's arguments filed 6/28/2006 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the impedance device in the present application is a tangible device) are not recited in the rejected claim(s). Although the claims are interpreted in light of the

specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant argues that Adachi never teaches or mentions to utilize an impedance device for reducing a difference between respective input voltages being input into the driver IC chip 108 and the driver IC chip 109. The examiner disagrees. In Fig. 3, Adachi teaches connecting an impedance circuit (206, 207, 209) between the driver IC chips 108, 109. The impedance circuit comprises a capacitor and resistors which change the voltage inputted into each driver IC chip 108, 109. Thus, the difference between respective input voltages being input into the driver IC chip 108 and the driver IC chip 109 is inherently changed.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis-Doon Chow whose telephone number is 571-272-7767. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dennis-Doon Chow
Primary Examiner
Art Unit 2629

D. Chow
November 22, 2006